A New Large-Signal Model Based on Pulse Measurement Techniques for RF Power MOSFET

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ABSTRACT

A large-signal model for RF power MOSFET has been obtained using a new characterization and extraction technique. This technique is based on pulsed I-V characteristics and pulsed S-parameters measurements, to take into account the thermal state of the device. A table-based model is used to represent the I-V drain current source. The complete large-signal model is implanted in an harmonic-balance commercial simulator and its accuracy is evidenced by a comparison with active load-pull measurements at L band.

I - INTRODUCTION

Power MOSFET technologies are of increasing usefulness for RF applications due to their robustness, simplicity and low cost, that make them suitable for personal communication systems. Performances of these technologies have been widely demonstrated, showing that they are at par with that of Silicon Bipolar transistors and GaAs MESFETs at L band frequencies (0.39-1.55 GHz), even for applications other than power amplification [1], [2].

Thus, it is necessary to develop accurate large-signal models for these new devices in order to use them in nonlinear circuits CAD. Classical semi-empirical models such as SPICE MOS level 3, are not well suited to model power MOSFETs that usually are assymetric structures (LDMOS,VMOS...) with short channel lengths [3]. In addition, power MOSFET behaviour is considerablely determined by thermal effects originated by device self-heating.

To avoid device self-heating effects during the characterization process, we propose a model based on a characterization of the transistor consistent with the thermal state of its normal DC operating point. The model is obtained by means of I-V measurements carried out under pulsed conditions. Our pulse I-V setup allows, at the same time, the achievement of pulsed S-parameter measurements that are used to obtain the voltage dependences of the complete large-signal model elements [4].

The drain current source is modeled using a new table-based interpolation technique that avoids some of the drawbacks of the classical spline representation.

A Motorola 4-cell LDMOS transistor, used in L band applications, has been characterized and modeled.

The complete large-signal model has been implanted in the commercial simulator LIBRA 4.0. In order to verify the accuracy of the model, active load-pull measurements have been performed for different operating classes (A, AB and B) and are compared with simulation results.

2 - CHARACTERIZATION TECHNIQUE

In power MOSFETs, thermal effects due to transistor self-heating can strongly influence device behaviour and should be considered carefully [5]. In fact, traditionals DC current/voltages characteristics present, at high DC power levels, an important decrease in transconductance, a negative output conductance and, generally, a fall in I-V curves caused by device self-heating [6]. Moreover DC I-V characterization do not allow to investigate the whole working domain of the device. Extraction procedures based on DC current/voltage characteristics could, in this way, lead to model inaccuracies.

Thus, it is necessary to have a I-V characterization consistent with the thermal state of the device in order to obtain a reliable power MOSFET model. Such a characterization is performed using a pulse I-V setup [4].

In our pulse I-V setup we have chosen a pulse width of 600 ns and a duty cycle of 1%. Both values ensure that the thermal state of the transistor is correctly controlled by the quiescent bias point.

Figure 1 shows the measured I-V characteristics of the tested LDMOS transistor, for a quiescent bias point of V_{ds} = 6 V , I_{ds} = 80 mA. We can observe the start of the breakdown effect for V_{ds} values over 35 V.

RF characterization has been carried out for devices mounted in test jigs by means of pulsed S-parameter measurements in the 1 - 3 GHz frequency range. Our pulsed I-V setup permits to acquire device S-parameters during the application of the short pulses starting from the quiescent bias point [4]. This procedure presents two major advantages with respect to multibias CW S-parameter measurements. First, it maintains thermal consistency in the transistor characterization and second, it allows the exploration of all operating regions (including high power and breakdown regions), thus providing a model in the whole range of control voltages.

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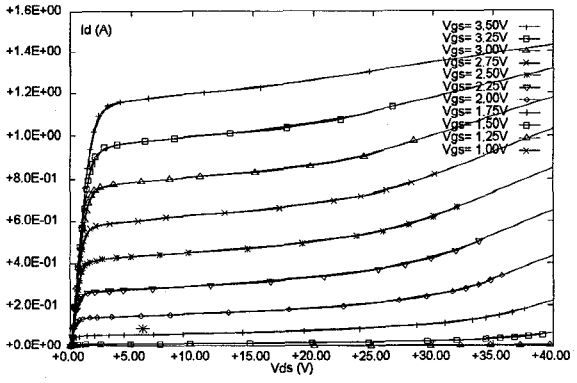

Figure 1 : Measured and modeled pulsed I-V characteristics of the LDMOS transistor. DC quiescent bias point : V_{ds} = 6 V, I_{ds} = 80 mA. Δ : measurement ; ---- : model

Moreover, cold S-parameter measurements (V_{ds} = 0, V_{gs} = 0) have been also carried out to extract the extrinsic elements of the model using the technique proposed by Lovelace et al [7].

3 - LARGE-SIGNAL MOSFET MODEL

We propose a classical FET topology for the power MOS transistors (figure 2). The drain current source is characterized under pulsed conditions with the transistor biased at its normal operating point. A time delay, Tau, is added to take into account the non-instantaneous response of the current source with respect to the V_{gs} control voltage.

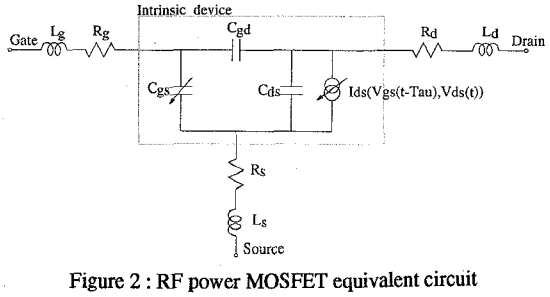

Figure 2 : RF power MOSFET equivalent circuit

The modelling of the drain current source is performed using a new look-up table model. This model is based on a piecewise parametric third-order Bezier polynomials [8] providing an interpolation-approximation spline representation of measured data. Convergence properties in an HB simulator as well as accuracy of the I-V model have been carefully checked. Figure 1 shows a comparison between simulated and measured characteristics illustrating the very good fit.

Extrinsic elements R_g, L_g, L_s, L_d are obtained from cold S-parameter measurements. The device tested is a four cell of 28 fingers LDMOS, so, the series resistances R_s and R_d are estimated to be very small, around 0.1 Ω [7]. Such low values are very difficult to be obtained from measurements. Therefore, we decide to set them to zero in the equivalent circuit.

A direct analytical method is used to extract intrinsic model elements C_{gd}, C_{gs}, C_{ds} and Tau from the intrinsic Y-parameters [7], [9]. Figure 3 shows the capacitances C_{gs}, C_{ds}, C_{gd} and the time delay Tau as functions of terminal voltages for the LDMOS transistor obtained from pulsed S-parameter with a quiescent bias point of V_{ds} = 6 V and I_{ds} = 80 mA. C_{gd}, C_{ds} and Tau present a nonlinear behavior only in the linear region of operation, while C_{gs} shows an important dependence with V_{gs} voltage. For sake of simplicity, only the dependence of C_{gs} with V_{gs} has been taken into account in the large-signal model. In fact, the use of a non linear capacitance C_{gs} improves significantly the simulated DC power consumption P_{dc}, as it is shown in figure 4.

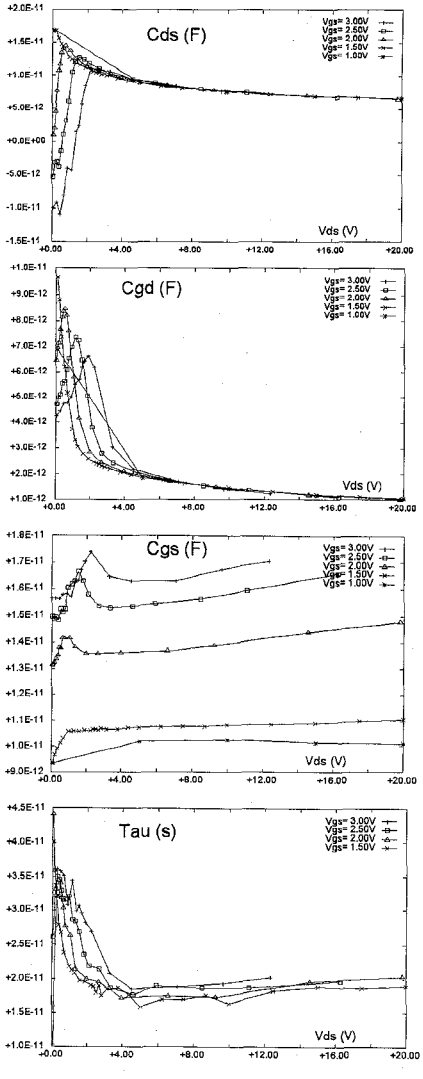

Figure 3 : Voltage dependence of C_{gs}, C_{ds}, C_{gd} and Tau of the LDMOS transistor. DC quiescent bias point : V_{ds} = 6 V, I_{ds} = 80 mA

4 - LOAD-PULL MEASUREMENTS AND MODEL VERIFICATION

Large-signal characterization of the LDMOS transistor has been carried out by means of an active load-pull setup [10]. The load-pull measurements have been performed at 1 GHz for three operating classes (A, AB and B). The goal of these measurements is to find the optimum load impedance values corresponding to the maximum performances of added power (A and AB classes) and power added efficiency (B class) for a given input power (16 dBm). Once the optimum impedances are determined, power transfer characteristics can be traced in order to validate the nonlinear model. The impedances presented to the harmonic frequencies were also measured to take them into account during the simulation process.

Our complete large-signal MOSFET model has been introduced in the harmonic-balance commercial simulator LIBRA 4.0, and the drain current source has been characterized with the pulse I-V setup for the same three operating classes (A, AB and B). Simulation of the three classes with their corresponding optimum impedances have been carried out. Figures 5, 6 and 7 show simulated and measured curves of added power and power added efficiency as functions of input power as well as the values of optimum load impedances. Figure 8 shows an increase of the gain for the B class measurements which is correctly predicted by the model. Figure 9 shows simulated and measured input impedance for the A class measurements.

The validity of our large-signal model is evidenced by the good agreement found between measurement and simulation for both low input-power and gain compression regions.

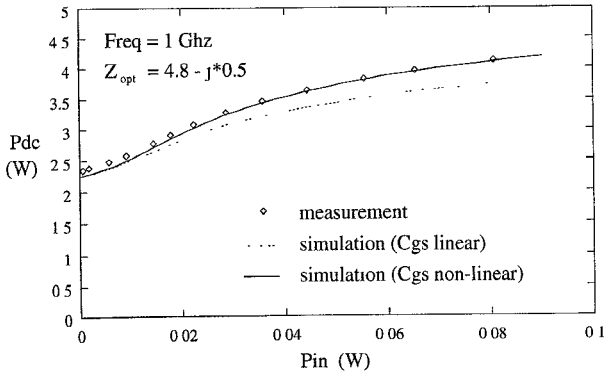

Figure 4 : A class (V_{ds} = 6 V, I_{ds} = 400 mA). Measured and simulated DC power consumption of the LDMOS transistor

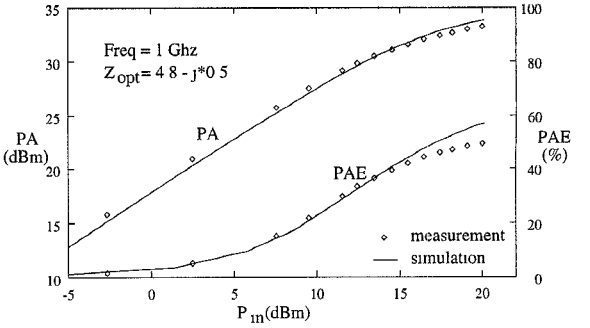

Figure 5 : A class (V_{ds} = 6 V, I_{ds} = 400 mA). Measured and simulated power added and power added efficiency of the LDMOS transistor

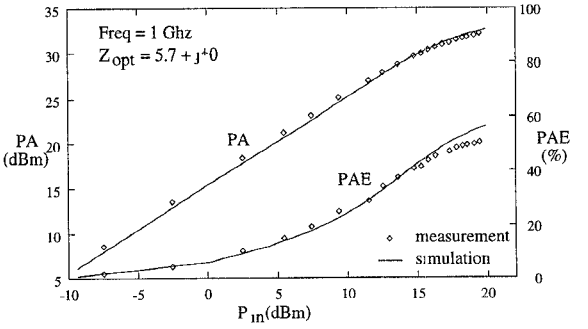

Figure 6 : AB class (V_{ds} = 6 V, I_{ds} = 80 mA). Measured and simulated power added and power added efficiency of the LDMOS transistor

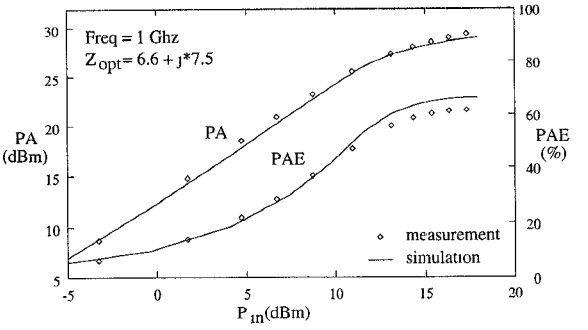

Figure 7 : B class (V_{ds} = 6 V, I_{ds} = 10 mA). Measured and simulated power added and power added efficiency of the LDMOS transistor

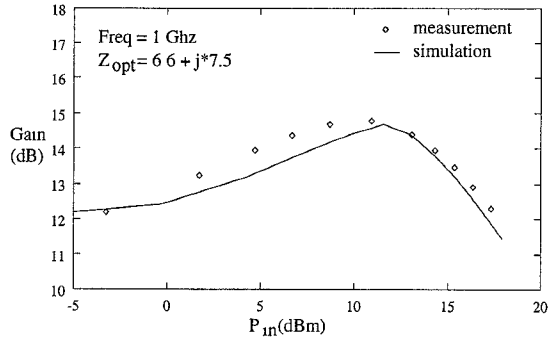

Figure 8 : B class (V_{ds} = 6 V, I_{ds} = 10 mA).
Measured and simulated gain of the LDMOS transistor

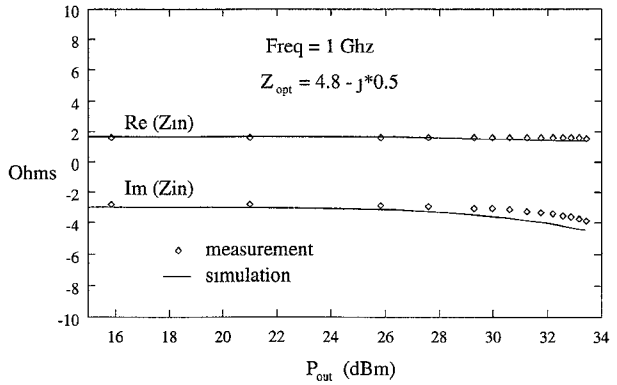

Figure 9 : A class (V_{ds} = 6 V, I_{ds} = 400 mA).
Measured and simulated input impedance
of the LDMOS transistor

5 - CONCLUSION

A new large-signal model for power MOSFET has been developed. It is based on a characterization consistent with the thermal state of the transistor normal operating point. This characterization is performed by means of pulsed I-V and pulsed S-parameter measurements. The look-up table drain current source model, which uses third-order picecewise Bezier polynomials, greatly shortens the modelling process and improves accuracy. Moreover load-pull measurements provide an invaluable tool for the determination of optimum load impedances and for the nonlinear model verification. Using such a tool a good accuracy has been found for various bias conditions (A, AB, B).

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REFERENCES

1 - N. Camilleri, J. Costa, D. Lovelace and D. Ngo - "Silicon MOSFETs, the microwave device technology for the 90's". IEEE-MTTs Digest, pp 545-549, 1993.

2 - J. Costa, D. Lovelace, D. Ngo and N. Camilleri - "Modeling a new generation of RF devices MOSFETs for L-band applications". IEEE-MTTs Digest, pp 293-295, 1993.

3 - C. Campbell, D. Detcher and T. Koenig - "Using IC-CAP/Saber to model power MOSFETs".
Characterization solutions - Hewlett-Packard, Winter / Spring 1994, pp 3-6.

4 - J.P. Teyssier, M. Campovecchio, C. Sommet, J. Portilla, R. Quéré - "A pulsed S-parameters measurement setup for the nonlinear characterization of FETs and bipolar power transistor". 23th EuMC 93 - Proceedings - MADRID (Espagne) - pp 489-493 septembre 1993.

5 - G.A. Hoile and H.C. Reader - "Nonlinear MOSFET model for the design of RF power amplifier". IEE Proceedings-G, Vol. 139, n° 5, October 1992.

6 - P.S. Barlow, R.G. Davis and M.J. Laserus - "Negative differential output conductance of self heated power MOSFETs". IEE Proceedings, Vol. 133, Pt I, n° 5, October 1986.

7 - D. Lovelace, J. Costa and N. Camilleri - "Extracting small-signal model parameters of silicon MOSFET transistors". IEEE-MTTs Digest, pp 865-868, 1994.

8 - J.J. Raoux - "Modélisation non linéaire des composants électroniques : du modèle analytique au modèle tabulaire parmétrique". Thèse de Doctorat de l'Université de Limoges, n° d'ordre 9-1995, 3 mars 1995.

9 - G. Dambrine, A. Cappy, F. Héliodoré and E. Playez - "A new method for determing the FET small-signal equivalent circuit". IEEE Trans. on MTT, Vol. 36, n° 7, pp 1151-1159, July 1988.

10 - Ph. Bouysse - J.M. Nébus - J.M. Coupat - J.P. Villotte - "A novel accurate load-pull set-up allowing the characterization of highly mismatched power transistors". IEEE Transactions On Microwave Theory and Techniques, Vol. 42, n°2, pp 327-332, February 1994.